Silicon Solar Cell Efficiency Increases Demonstrated by Thermal Process Optimization in the Metallization Process

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Introduction

The solar industry’s drive toward lower cost per W requires both lower cost as well as higher solar cell efficiency. The relationship between an optimized thermal process and increased cell efficiency has long been known, although the quantification of this relationship and the method to achieve it have been less well understood. This article outlines the method of process optimization, and it measures the resulting cell efficiency improvements as they relate to volume production of solar cells. The basic strategy used is applicable for a variety of thermal processes, both within the silicon as well as thin film solar cell manufacturing. This article, however, focuses on the silicon solar cell metallization process.

Experiment Overview

As a manufacturer of silver pastes for solar cell applications, Heraeus has worked on perfecting its material’s performance in the metallization process for some time. A design of experiment using KIC’s e-Clipse thermocouple (TC) attachment fixture was developed to use more sophisticated thermal profiling and process optimization tools to help identify the very best wafer profile for the company’s latest paste, and to measure what impact such process optimization would have on cell efficiency. A number of identical wafers were processed in a metallization furnace under different thermal process conditions, and their resulting cell efficiency improvements were measured. The results are presented in this article.

Cell Metallization

For solar cell metallization applications, thick film paste is a suspension of a functional (conductive) phase, binder, vehicle and additives. Silver is the most common conductive filler used for front contact paste. The binder is composed of a glass frit that is used to bind the functional phase to the silicon wafer. Specialized chemistry of the binder also is required to etch through anti-reflective and passivation layers, and initiate effective ohmic contact between the silver and silicon. The vehicle is an organic composition that provides printability of the pastes and is composed of resins, solvents, and modifiers. The resins support the solids of the other phases and keep them in homogeneous suspension. Solvents are used to dissolve the resins, and they must be stable in production conditions. These organic components of the paste must burn off cleanly in the fast-firing process so as not to contaminate the surface of the wafers or introduce sources of recombination near the p-n junction.

The paste is applied using the standard screen printing process common to crystalline silicon solar cell production. After printing, the wafers pass through an in line dryer and proceed directly into the firing furnace. Most furnaces today contain six firing zones, but the differences from manufacturers come from the length of the zones and how they maintain a uniform firing environment within the furnace.

The thermal process of the wafer is one of the keys to achieving improved efficiencies. Drying steps are expected to remove most of the solvent used in the pastes before entering the firing zones. Solar cell metallization generally follows a spike profile type. Wafers only see peak temperature for approximately 1-4 seconds based on wafer and metallization chemistries. The most important steps include the clean burnout of the organics in the paste followed by etching through the silicon nitride (or other) passivation/ARC layer and, ultimately, the formation of good ohmic contact between the sintered silver and the very top layer of n-type silicon. These all lead to low contribution from series resistance and recombination resulting from the formation of the contacts. Control of this profile will become more crucial as the emitter depth decreases with increasing sheet resistance. Both uniformity of diffusion and furnace will be necessary to achieve the desired efficiency improvements.

Thermal Process Development

Since the hypothesis is that the wafer's thermal profile will significantly impact the cell efficiency, an experiment was designed to vary the wafer profiles while keeping all other variables constant:

Wafers: We purchased a large quantity of wafers that were known to be of a very consistent quality

Aluminum coating: All the wafers had consistent aluminum coating.

Silver paste: The Heraeus paste SOL 9235H was from the same batch consistent.

Screen print: Great care was taken when screen printing the Heraeus paste to secure that the paste deposition, line width, and line thickness were uniform across all wafers.

Profiling: All profile measurements were taken with a high accuracy thermal profiler that used a new TC attachment fixture that was proven to offer accurate and consistent readings on the surface of the wafer. The type K TCs in the fixture used a flattened disk bead rather than the spherical bead for added accuracy and repeatability

Efficiency Testing: The solar simulator was a continuous lamp tester used in all measurements.

Image 1: Heraeus silver paste

The base line profile on these wafers had been developed prior to the project based on extensive knowledge of the paste chemistry and years of practical experience with the metallization process. The base line profile can be seen in dark blue in Figure 1. For the base line test, as with all the subsequent process improvement tests, the wafers were processed at the same time and fired under the same conditions. Ten wafers were run through the furnace within a short period of time, and all were subjected to the same profile. After firing, we measured the cell efficiency in our continuous lamp tester. The average efficiency for the base line profile was 15.53 percent, as can be seen in Figure 2 (η Cell). Based on the type of wafer that was selected for this study, and the fact that a continuous lamp tester was used rather than a flash tester, this efficiency number was considered good. Now we wanted to make it better.

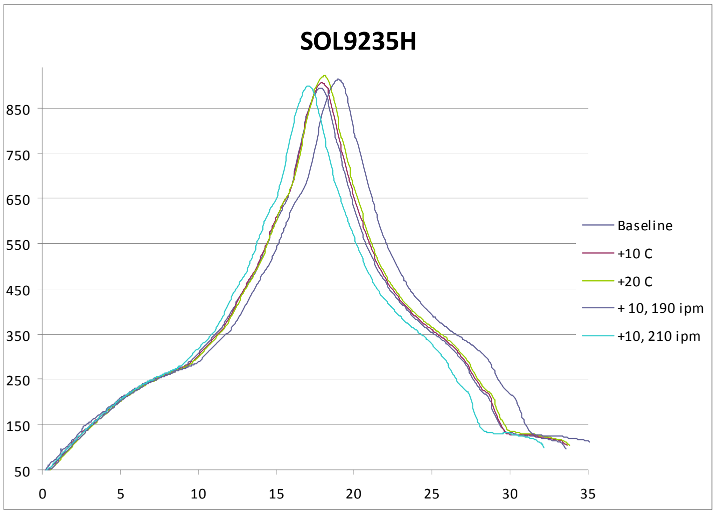


Figure 1: The wafer profiles for each group

It is important to acknowledge that what we were trying to accomplish was not to find a single "golden" profile for the wafers, but rather the optimal thermal process window. The Heraeus paste SOL9235H is a very robust paste that can perform well throughout a range of profiles. Establishing a thermal process window will set the upper and lower limits for the wafer's peak temperature, time above certain temperature levels, etc. within which the cell efficiencies will be highest.

	Jsc	Voc	FF	η Cell	Imp	Vmp	Pmax	Rs	Rsh
Group 1 Base line	32.572	0.6193	76.97	15.53	7.380	0.5120	3.779	0.00611	9.8
Group 2	32.727	0.6219	78.25	15.93	7.467	0.5192	3.877	0.00576	10.6
Group 3	32.658	0.6192	78.20	15.81	7.437	0.5175	3.849	0.00580	9.4
Group 4	32.907	0.6234	78.17	16.04	7.512	0.5195	3.903	0.00568	8.7
Group 5	32.818	0.6202	78.02	15.88	7.472	0.5173	3.866	0.00579	10.0

Figure 2: Cell efficiency testing

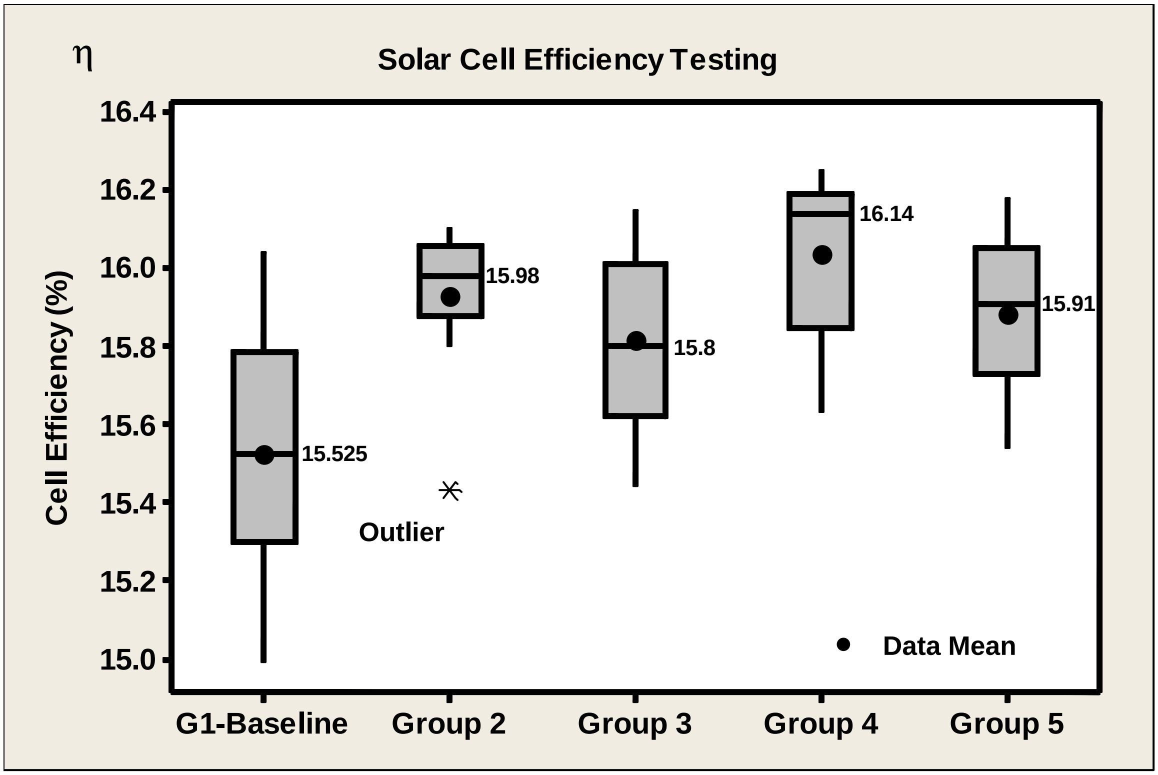
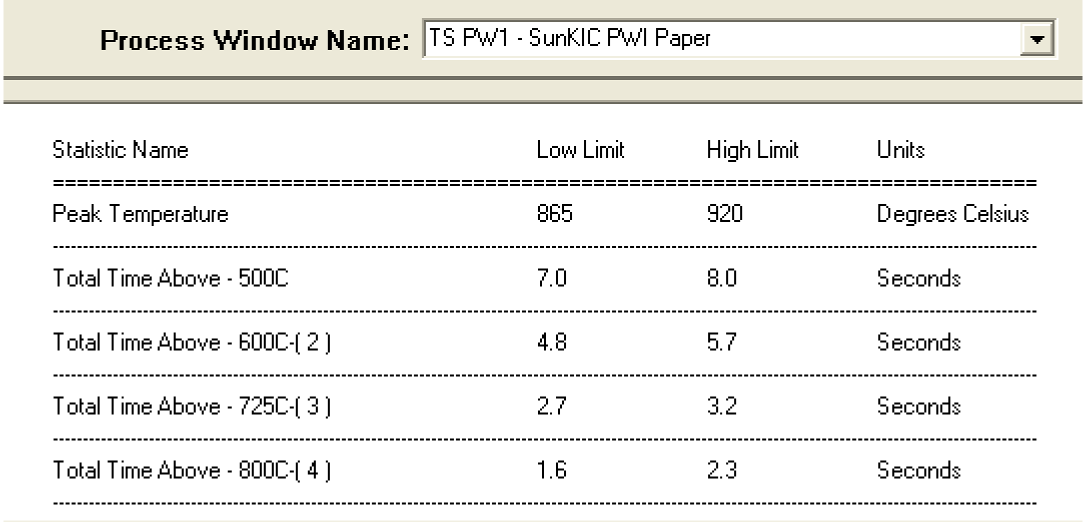


Figure 3: Boxplot of cell efficiencies for base each wafer profile

Since we did not yet know the upper and lower limits to our process window, we used the base line profile as a starting point, and we initially set relatively wide process limits around it as shown in Figure 4. The profiler software always measures how well the profile fits the chosen process window with a single number called Process Window Index (PWI). The PWI number is 100 percent when the profile is at the edge of the process window. The lower the number, the closer the profile is to the center of the process window. A PWI of 0 percent represents a profile at the very center of the process window.



Process Window Name: TS PW1 - SunKIC PWI Paper

Statistic Name	Low Limit	High Limit	Units
Peak Temperature	865	920	Degrees Celsius
Total Time Above - 500C	7.0	8.0	Seconds
Total Time Above - 600C-(2)	4.8	5.7	Seconds
Total Time Above - 725C-(3)	2.7	3.2	Seconds
Total Time Above - 800C-(4)	1.6	2.3	Seconds

Figure 4: Original Process Window

Our profiler also has profile simulation software that allowed us to change the furnace zone temperatures or conveyor speed in the software, and to immediately predict the resulting wafer profile. For the first process improvement step, we suspected that a higher peak temperature would benefit the metallization. We tried a few zone temperature changes in the software and studied the software simulation of the corresponding profile before settling on a 10°C increase in the furnace peak zones (Zone 5 and 6). Once the furnace stabilized on the new settings, we ran a set of 10 wafers for our Group 2 test. The average cell efficiency increased from 0.40 to 15.93 percent. For Group 3, we increased the peak temperatures settings in zones 5 and 6 another 10°C, but the average cell efficiency of the 10 wafers dropped by 0.12 percent.

For the Group 4 test, we set the zones back to the Group 2 level and reduced the furnace conveyor speed. The prediction software showed the impact on the wafer profile both in terms of peak temperature changes and, in particular, in terms of time above the various temperature levels shown in Figure 4. Due to this, we reduced the conveyor speed from 200 to 190"/min. The average cell efficiencies increased yet another 0.11 percent above the Group 2 numbers to a cell efficiency of 16.04 percent. Our final test for Group 5 kept the temperatures stable but increased the conveyor speed from 190 to 210"/min. That dropped the average cell efficiency by 0.16 percent.

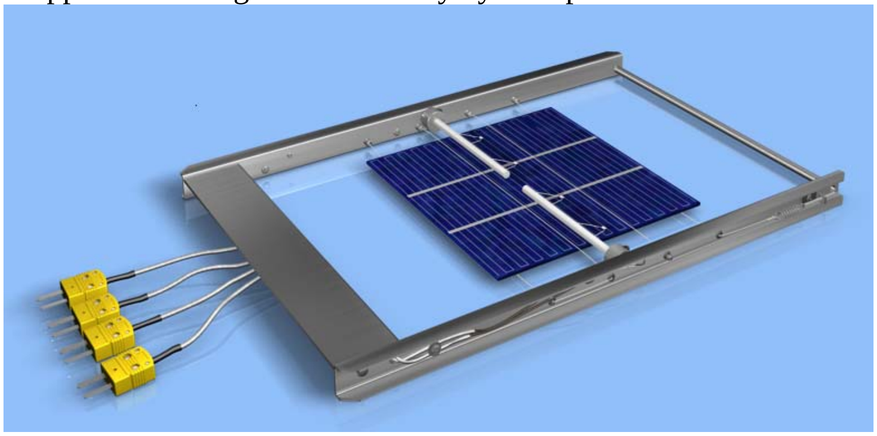


Figure 4: e-Clipse TC attachment fixture

Conclusion

By systematically changing certain key profile dimensions, such as peak temperature and time above 500°C, we were able to identify the “sweet spot” in the metallization process. The PWI index and the profiler’s simulation software allowed us to quickly identify the appropriate furnace settings for profiles below, above and in the middle of the optimal settings. This sweet spot yielded an average cell efficiency of 0.51 percent higher than previous experiments had allowed.

The Heraeus SOL 9235H silver paste’s properties allow for high-efficiency processing in a range of profiles, hence a process window can be established around the “ideal” profile identified above. Heraeus now advices its clients to the appropriate process window for each application.

With modern profilers, solar cell manufacturers can adjust their furnace setup until the wafer profile is positioned within the suggested process window. Over time, the thermal process will drift due to a number of variables such as heating lamps changing as they get older, wear and tear in the furnace, conveyor speed drifts, exhaust changes, and more. It then is a simple task for the manufacturing engineer to run another profile, and to use the profiler process optimization software to identify the furnace settings that will yield the appropriate profile.

This method for process optimization depends on accurate and repeatable profile readings. One excessive noise in the profile readings historically has been caused by the attachment method for the TCs. Both cemented and dummy wafer TCs tend to measure the material used to secure the TCs in place, rather than to measure the surface of the wafer. Pinning the TC to the wafer with a weight suffers from non-repeatability. The fixture with flattened TC beads has worked well for us.

Finally, process optimization must be quick and easy enough to be useful for volume production lines, as opposed to only the laboratory line. There is little use in perfecting the process in the laboratory just to see the transfer to the production lines fail because the furnace properties are different. Once the correct process window is established, the high-volume furnaces can be adjusted within minutes, keeping production downtime to a bare minimum. This task must not only be performed during transfer from the lab to the production line, but it also must be performed periodically due to the drift in the thermal process that is a fact of life in any production line. The few minutes it takes to adjust the production furnaces for peak performance is richly rewarded by the ability to consistently produce higher efficiency cells.

Future Studies

The temperature readings taken by the e-Clipse TC attachment fixture are higher than historic readings taken by older TC attachment methods. A future study will focus on quantifying the accuracy and repeatability of the new profiling method as it relates to the theoretical true wafer surface temperatures.