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Wafer Bumping for Flip Chip Attach

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There are five commonly used methods of wafer bumping for flip chip attach, three of which are challenging and expensive: Stud bumps formed by ball bonding using gold wire; plated gold bumps using electrolytic or electroless gold; and plating solder bumping by electrolytic or electroless solder plating. The remaining two of these five methods of wafer bumping are getting a great deal of attention recently: solder ball bump placement and reflow and printed solder bumping using screen printing of solder paste by stenciling and reflow.

Manufacturers producing wafer bumped die are fine-tuning this evolving process continuously. One area that requires improved process development and process control is the thermal process. To produce higher yields at lower costs on a regular basis, it is imperative to eliminate all defects associated with each step of the manufacturing process, including the reflow process. The requirement for traceability of each lot of wafers is on the rise, adding significant cost to production. Automating this process will reduce this cost considerably.

As the trend toward larger wafer sizes continues, product cost also increases. Those potential problems associated with the thermal process on wafers of 100 to 200 mm still pose problems with the 300 mm, and it has become crucial to catch these problems before they can affect the product. There are several ways to ensure that the 100- through 300-mm wafers are processed optimally for high quality and volume as well as maintaining these standards throughout production. A three-step program is commonly implemented for the development of the process. Once developed and optimized, the second phase—maintaining process control—will become easier.

Define the Process

Depending on the material used, for example, 63Sn/37Pb, 90PB/10Sn, Sn/Ag(3.0)/Cu(0.5), each has an individual specification. The recommended process window may vary by alloy and supplier. This window may even be much smaller when using materials such as lead-free and high-lead solders. All these specifications are key when considering what will affect bump quality and appearance. Figure 1 shows the process window for one of these materials.

Process Window

Solder Paste: Heraeus F10 Sn63Pb37 NC or N

Statistic Name	Low Limit	High Limit	Units
Max Rising Slope (Target=1.5) (Calculate Slope over 20 Seconds)	1.0	2.0	Degrees/Second
Time Above Reflow - 183C	30	60	Seconds
Peak Temperature	213	233	Degrees Celcius

Figure 1. Define the process window.

Measuring and Analyzing the Existing Setup

To measure how well a recipe meets the requirements to achieve the established specs, one must first run a profile (Figure 2). The analysis of this information is done in several ways. Most favor a scientific or mathematical analysis rather than a subjective analysis. By assigning a numeric value to each result, i.e., the time and temperature readings of each thermocouple, an instantaneous answer is displayed, thus automating this step. This is done by ranking process profiles on the basis of how well a given profile "fits" the critical process statistics. A process window index (PWI), as shown in Figure 3, is a measure of how well a profile fits within the user-defined process limits. The center of the process window is defined as zero and the extreme edge of process window as 100 percent. This allows a numeric value to indicate what percentage of the process window is being used (Figure 4).

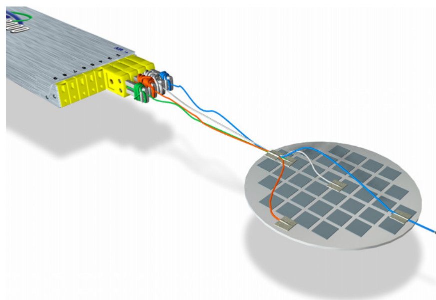

Figure 2. Thermocouples (TC) attached to wafer.

Optimizing the Process

In the example in Figure 1, the center or target for each of these specs is:

- Max rising slope: 1.5°/second
- Time above reflow: 45 seconds
- Peak temperature: 223°C

To ensure a process within some of these critical parameters, the optimum recipe must be determined so that it is centered within the process window. This will allow for slight shifts in the oven without causing potential defects, such as those seen in Figure 5. There are billions of alternative combinations of belt speed and zone setpoints. It is advantageous to use existing software that will find the correct recipe quickly and accurately. These will take into consideration the specific oven and correlate this information to the process window and wafer.

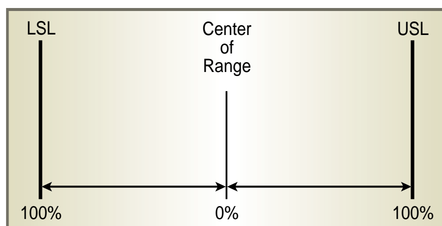

Figure 3. The process window.

Finding the optimum setup will increase the percentage of first-pass yield. When optimizing the process, it is important to look at each specification as it relates to potential problems. One typical area of concern is wettability. Insufficient wetting is directly related to the thermal process. Ensuring appropriate wettability is imperative to the formation and quality of good solder balls. Excess soak time may lead to depletion of flux, hindering wetting. Some are looking to eliminate the soak portion of the profile and use a continuous ramp to peak. Insufficient time over liquidus may not allow the bumps to form properly and could cause an unacceptable cosmetic appearance. Cooling is becoming a focal point as well. All these factors add to the many variables in finding the correct process window.

Maintaining Process Control

Any change to the conditions of the oven from its initial setup opens the possibility of defects. Because many companies are trying to maintain Six Sigma manufacturing processes, it is imperative to catch the potential problems before they happen. Additionally, defects caught post-reflow may not be repairable, or the cost may be high.

Wafer cost can be extremely high by the time it reaches the thermal process. Therefore, it becomes important to avoid any defects at this stage and immediately take corrective action if the process is no longer in control. Although a modern reflow oven will monitor its own settings, it is equally important to monitor the actual process—the wafer's time temperature profile.

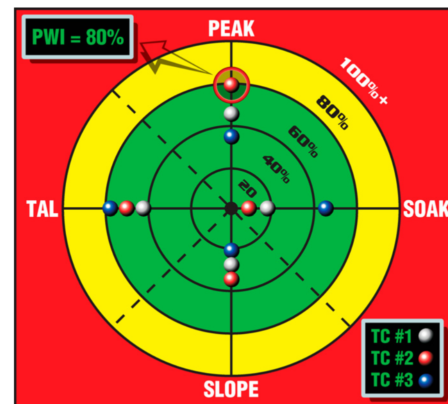

Figure 4. The process window index (PWI).

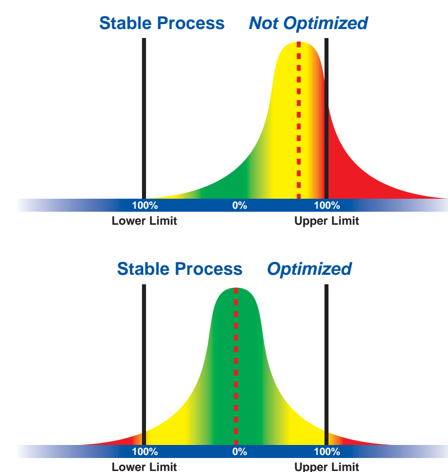

Figure 5. Optimize the process.

Heater failures, fan system malfunctioning, changing oven properties due to flux build up, preventive maintenance, varying exhaust settings, non-stable conveyor speed and more all affect the wafer profile negatively while the oven controls may not catch the emerging problem. In other words, a process is out of control and no information is available to take corrective action. Each potential problem brings with it its own set of defects. Once in production, the user must be assured that all the wafers are seeing the optimum process that was established.

Traceability and Protection: SPC & Cpk

Creating statistical process control (SPC) charts of the profiles of the wafers is the first step in using process capability (Cpk) as a method of determining PWI changes and issuing an alarm. A continuous process monitoring system with independent thermocouples can automatically and in real-time calculate the profile for every wafer being processed. Such continuous process data also may calculate the Cpk for each wafer.

In Figure 6, the SPC charts indicate that there is a warning of a Cpk that is less than the defined 1.33 acceptable minimum. This indicates that while product is still being processed in spec, the probability of the next product being produced in spec is lower than the acceptable minimum number. This would produce a warning so that action may be taken prior to an out-of-spec condition. This is a proactive approach to Six Sigma. Should the current condition continue to drift and an out-of-spec situation occurs, an alarm will be made.

SPC charts also provide traceability of the lots. Documenting the various processes that the wafer goes through may add cost; however, it is becoming a requirement rather than an option. Automating this process has numerous advantages, such as:

- Reducing the risk of defects
- Reducing the costs associated to data collection
- Allowing the use of these charts on a continuous basis for process control
- Providing traceability for all lots

Figure 6. Statistical process control (SPC) charts with process capability (Cpk) values.

Conclusion

While the pre-reflow processes for wafer bumping are critical for attaching flip chips, emphasis continues to be placed on the reflow process. This area is key to reducing the cost of ownership. The specifications for various materials on larger wafers continue to change and be fine-tuned, often resulting in tight process windows. It is imperative to accurately and optimally create a recipe that provides higher yields at lower costs. Continuous monitoring is the key to ensuring that all products are built within the specified process window. Automated traceability provides customers with assurances that all their products meet their requirements of zero defects.

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