Improved Thermal Process Control for Lead-free Assembly

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Introduction

The impending shift to lead-free electronics assembly has raised several serious issues, including the projected need to increase the thermal tolerances of electronic components. SnAgCu, with a eutectic of ~217°C, currently appears to be the preferred alloy in the US and Europe. It is projected that with this alloy, reflow process temperatures will need to rise to a peak of 260°C. The current maximum thermal tolerance for most electronics components is commonly agreed to be 235-240°C.

The NEMI Lead-free Roadmap calls for an increase in component tolerances to 260°C. This proposed 260°C maximum process temperature is based on current industry practice, which calls for a process window of at least 30°C to ensure proper reflow of all solder joints on the PCB. While it is probable that most components will eventually be built to this proposed standard, this transition will take many years. Electronics assemblers implementing lead-free processes will be faced with serious issues during this transition, issues that may continue to linger well past the time when market forces have made lead-free assembly essential.

One solution to this problem that has not been investigated is narrowing the thermal process window. The proposed 260°C maximum process temperature is based on current industry practice, which calls for a process window of at least 30°C to ensure proper reflow of all solder joints on the PCB. It has been proven that electronic assemblies can be reliably reflowed in reduced process windows.[1] The purpose of this paper will be to establish that lead-free electronic assemblies can be successfully soldered in a reduced process window, thus offering the potential to limit the impact of the recognized need for an increase in component thermal tolerances. The experiment will utilize new profiling software that is capable of centering the product thermal profile precisely in the process window, given a sufficiently capable and flexible reflow oven. The application of this technology may provide an answer to one of the most critical problems raised by lead-free electronic assembly.

Current Lead-Free Status

Little has changed in the last year, other than increased industry acceptance of the eventuality of lead-free electronic assembly. At recent industry meetings (IPC Works 2000, SMTAI 2000) there has been significantly less grumbling about “why” and many more questions about “how”. It is almost certain that lead-free electronic assemblies will be mandatory by 2008 in Europe, and Japan’s effort for voluntary compliance appears to be on schedule (2002: General use of lead-free solders in new products; 2003: Full use of lead-free solders in all new products). The majority of major cell phone manufacturers are far along in developing lead-free units, and most major automotive manufacturers are working towards lead-free (except for the battery) vehicles. It is doubtful that there will be lead-free legislation in the United States. The consensus in the American Electronics industry is that lead-free is coming, albeit slower than initially expected, and the shift will primarily be due to market forces. Consumer electronics are expected to transition first, with high reliability applications following as the technology is proven. As the papers in this session indicate, a great deal resources have been devoted to researching the issues associated with the transition to lead-free assembly.

Lead-Free Process Issues

Currently available lead-free solders have a solidus/liquidous point about 20-50°C higher (depending on the alloy) than the lead-based pastes currently in use. The primary challenge lead-free solders will present electronics

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[1] *Delott, Charles R. “Thermal Process Optimization and Monitoring for Long-term Product Reliability” Circuits Assembly, May 2000*

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assemblers with is higher process temperatures. The current thermal process window is a wide one. The melting point of eutectic Sn63/Pb37 solder is 183°C, and 200-205°C is the most common lower temperature limit for reflow. The upper limit is generally 235°C, which is the maximum temperature that some sensitive components can be exposed to. These high and low process limits provide a Delta of over 30°C—wide enough that a carefully monitored process can be expected to produce low defects and high yield with little fear of defects caused by process drift.

SnAgCu, the most prevalent lead-free alloy in the United States and Europe, has eutectic temperature of 217°C. Current research (see below) indicates that this alloy needs to see a minimum peak reflow temperature of 230°C. With the component tolerances specified in the NEMI Lead-free Roadmap of 260°C, the result is a similar 30°C process window. In fact, the NEMI component tolerance specification will be difficult to attain, at least in the near future, and will present a significant challenge for component and board manufacturers for several years to come. Lasting component shortages make it obvious that suppliers are running at full capacity, and it is uncertain where the resources to produce components with increased thermal tolerances will come from. Additionally, it is reasonable to assume that 260°C will be a worst case process limit, and components produced for this limit will not have the safety margin current components for lead-based assembly have at the 230-235°C limit.

Even if components perform satisfactorily after being exposed to a 260°C peak reflow temperature, there are many compelling reasons to limit the reflow temperatures an assembly is exposed to. Minimizing process temperatures limits the thermal stress on boards and components, reducing the potential for manufacturing defects. Higher reflow process thermal cycles expose PCB's to significant amounts of stress on plated through holes and barrels, which can lead to cracking. Higher first pass temperatures on double-sided assemblies exposes bottomside finished surfaces to oxidation or interdiffusion, which in turn can lead to solderability problems on the second pass. Limiting peak temperatures limits intermetalic growth, especially on topside components that are exposed to two passes, and also limits the potential for the popcorning of components with high moisture content. Increasing the maximum reflow temperature is expected to increase the moisture sensitivity of plastic packaged components.

The problem of narrow process windows will be further exacerbated by the trend to more complicated assemblies with increased component density. Finding a profile that will reliably reflow these assemblies, especially larger ones that can experience large peak temperature differentials across the board, has never been easy. Real world production issues like maintaining high throughput and minimizing oven changeover times between production runs also figure into the equation. The Lead-free challenge will be to find and utilize technology that will allow electronics assemblers to define and maintain optimal thermal processes in the drastically reduced Lead-free process window. The increase in peak process temperatures, combined with the trend to components of decreasing size and robustness, means that precision tools will be required to find profiles that will safely process product at the higher temperatures required by lead-free solder.

New Technology for the Reflow Process

The current method of profiling conveyorized thermal processes is to attach thermocouples to a product, and, using a wireless device or data-logger, run the device and the product through the oven to record the product thermal profile. This is typically done on a regular basis to verify that the oven is working correctly, whenever the oven is changed over, and when a new process needs to be set up. There are several problems with the status quo:

- Profiling is time consuming, and can become even more time consuming if the data is lost, for example, through a bad download, and another profiling run is required.
- Current profiling software is complicated and requires several hours of training to ensure operator competence. Setting up a profiler is also complicated, and has to be repeated for each new oven the profiler is used on.
- Oven setup is a matter of trial and error, with multiple profiling runs being required to find an acceptable profile for new products. For a tight lead-free process window, it will be very difficult to find an acceptable profile using conventional profiling technology.

The next generation profiler features a more robust hardware configuration than conventional profilers and a totally redesigned software platform. The new configuration guarantees a perfect profile every time with a new wireless download. The next generation profiler provides data in real-time as it passes through the process and simultaneously records the data internally. When the profiler has completed its run through the process, the internally logged profile is automatically wirelessly downloaded, filling in any gaps that may have occurred due to broken transmission of the real-time profile. This new feature ensures that every profile run is a good one, and that it will never be necessary to hold up production to repeat a profile due to data loss.

The new software features minimal initial setup and a radically simplified operator interface that eliminates tedious board mapping. The software is designed to be completely intuitive and require very little training. It comes with an updateable database of hundreds of popular solder pastes, which allows the operator to automatically select the specs for the paste being used. A series of screens with clear explanatory graphics steps the operator through the profiling process from beginning to end, and if the profiling is being done with one of the selected ovens that communicate with the software, the software automatically changes the oven setpoints to the approved profile.

Figure 1: Simplified Software Startup Screen

A significantly improved automated prediction tool allows users to predict how changes to belt speed and oven setpoints will affect a product profile. The software option can create and evaluate *billions* of potential oven recipes, automatically selecting the recipe that best fits the process window in about a minute. The automated prediction tool is designed to center the profile in a process window designated by the user, who may set limits particular to their processes. An example of this is the profiles mentioned in the section on lead-free solders above—if the assembly can't see temperatures below 230°C, or above 260°C, the automated prediction tool will find a profile that will be centered between the high and low limits if the oven is capable of achieving one.

Wetting Issues

One critical factor in finding optimal profiles for the Sn3.8Ag0.7Cu alloy used in the profiling experiment was setting the lower process limit. Wetting balance testing of the alloy was conducted with a variety of common lead finishes: nickel/gold; silver; pure tin; OSP; and palladium at temps from 230-255°C. The purpose of the testing was to determine at what temperatures each finish can be safely reflowed with good wetting.

In a wetting balance measurement, the instrument records the dynamic wetting force as the solderable surface is dipped into the molten solder. In the operation of a wetting balance test, the specimen is suspended from a sensitive balance and immersed edge-wise, at a predetermined and controlled rate, and to a specified depth, into the molten solder maintained at a controlled temperature. As a result of the interaction between the molten alloy and the board finish, the wetted coupon is subject to time variant vertical buoyancy forces and downward surface tension forces. The forces are detected by a transducer and are converted into an electrical signal, which in turn is recorded by the data acquisition system in a computer.

The specimen is first dipped in flux, attached to the balance, and then immersed in the molten solder to a specified depth by raising the solder bath. The coupon is then held in that position for a specified period of time. The test ends by lowering the solder bath. The force experienced during the wetting is recorded and plotted as wetting force vs. time. A characteristic wetting curve is shown in Figure 2.

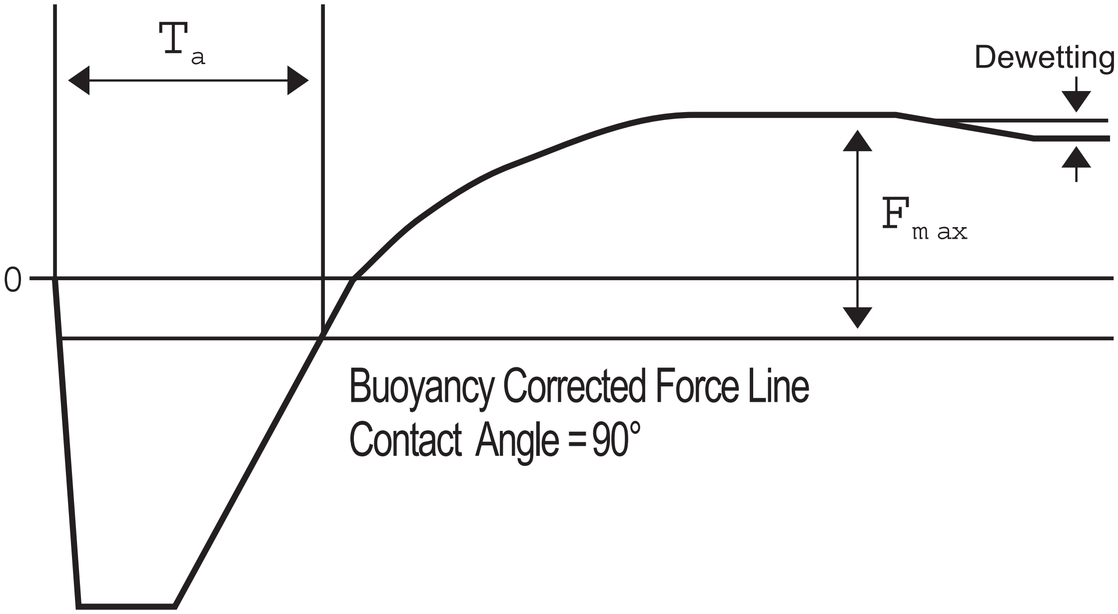


Figure 2: Characteristic wetting force vs. time graph.

The key wetting balance parameters measured were T_a and F_{max}. T_a is the time to the buoyancy corrected force line. At this time the solder contact angle to the test coupon is 90^o and the wetting forces pulling the coupon into the molten solder equals the buoyancy force pushing the less dense coupon out of the molten solder. F_{max} is the maximum wetting force exerted by the solder on the coupon and is directly proportional to the height the solder climbs up the coupon.

A Multicore Universal Solderability Tester (MUST II) was used in the experiments. The wetting balance tests were conducted in accordance with the standard IPC J-STD 003. The solder alloys were brought to within ±1°C of the specified test temperature. The coupon was dipped in flux for a 5 seconds and the excess flux was drained off. After fluxing, the coupon was placed on a mounting clip and placed on the wetting balance. Any dross that may have formed on the solder was wiped away from the molten solder surface prior to coupon dipping. The coupon was then dipped into the molten solder at a constant speed of 20 $mmsec^{-1}$ to a depth of 5 mm. The total immersion time was 10 seconds. At the end of 10 sec, the solder bath was lowered and the coupon removed from the clip. The testing was carried out in air. Seven specimens were tested for each flux/finish/solder alloy combination.

The data acquisition software collected data points every 0.001 sec for the test duration. Wetting curves resulted for the wetting force vs. time, with extracted values for wetting time (T_a) and maximum wetting force (F_{max}), measured relative to the buoyancy-corrected zero force line. Measurement with respect to the buoyancy-corrected zero force line and not to the instrument zero force line allows the data obtained to be independent of the sample size and shape.

The wetting time and maximum wetting force as measured by a wetting balance is a function of both the PWB surface finish and the solder temperature. The time to neutral buoyancy force, T_a, for a Sn3.8Ag0.7Cu solder alloy with a number of common lead-free surface finishes and solder dip temperatures is plotted in Table 1. A commercial no-clean flux was used. The wetting time is seen to decrease with increasing temperature, however, the rate of decrease declines above 240^oC.

The maximum wetting force, $F_{max,}$ is a measure of the force exerted on the coupon by the molten solder pulling it into the solder pot. The surface finish has a significant effect on F_{max}, but in general, the change in F_{max} with temperature is relatively small above 240^oC (Table 2).

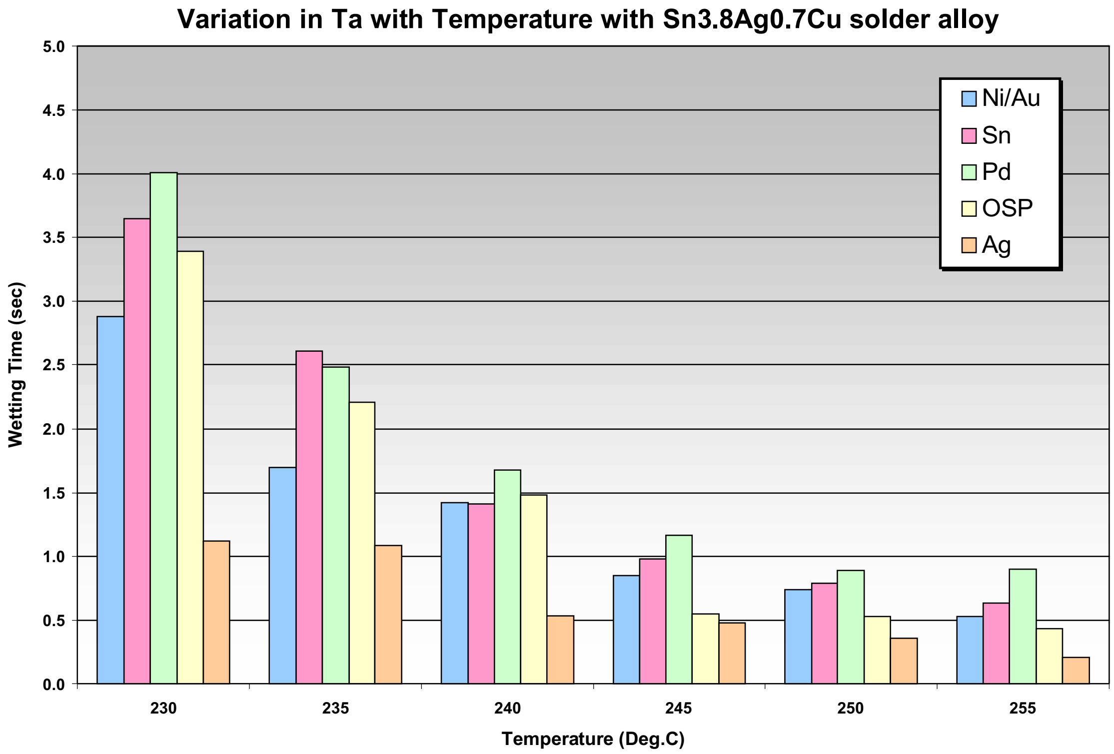


Table 1: Wetting Test Results: Variation in Ta

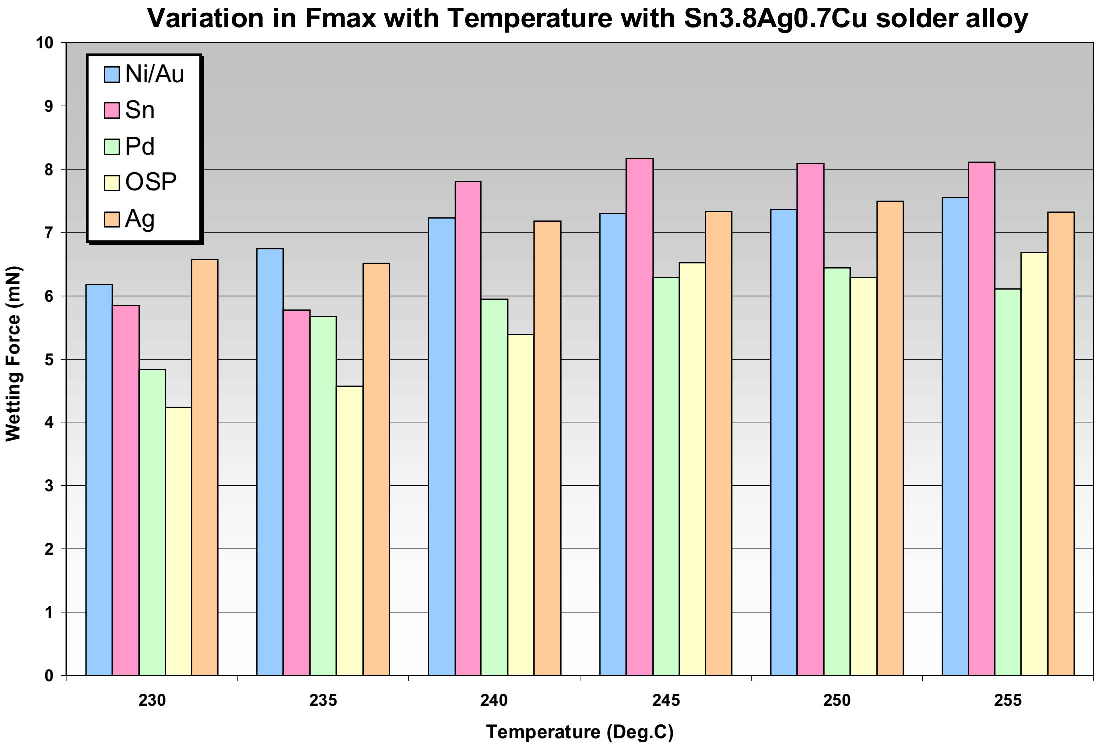


Table 2: Wetting Test Results: Variation in Fmax

With the exception of the OSP, adequate wetting was achieved at temperature of 230°C and above. Increasing the temperature to 235°C significantly reduced the wetting time for most of the finishes. For the reflow profile in the profiling experiment detailed below, a temperature centered around 237.5°C was selected to maximize wetting while minimizing the thermal exposure of the SMT components and the PWB.

Board Ranges

In developing a thermal profile for an electronic assembly, critical factors are the size of the assembly, the density of the components on the board, and the mix between large heavy components and lighter ones. Generally, the greater the contrast in component densities, the tougher it is to develop a profile for the board. This is because small components will naturally heat up more rapidly and be heated to higher temperatures than heavier ones. The difference between the hottest component on the assembly and the coolest is referred to as the Delta Temperature (ΔT). Minimizing the Delta Temperature on a given assembly during the reflow process is the key to developing an optimal profile.

Temperature differentials across the board will be a critical factor in whether a board can be successfully processed with lead-free solder. With a sophisticated profiling system, it will be relatively simple for smaller boards mounting components with consistent thermal mass to make the transition to lead-free. More complex assemblies with a large mix of components offer a more difficult task, as the temperature differential across the board may push the temperature of lighter components past their thermal stress limit while the densest components may fail to reach an adequate wetting temperature.

In terms of profiling difficulty, electronic assemblies range from cell phone boards and other light consumer products, which are relatively simple to profile, to automotive boards, motherboards, and large heavy duty server and switching boards, which can be very challenging to profile.

Test Vehicle

The test vehicle for this experiment was an automotive transmission controller currently in production using Sn/Pb eutectic solder. It is typical of future assemblies that must be compatible with lead free processing. The test vehicle is an underhood application that currently has a maximum operating temperature of 125°C. Board dimensions are 5.5"x7.6", with 4 layers and an overall thickness of 0.062". Components on the board include a large 96 pin through-hole connector off-set from the center of the board and running nearly the length of the board; up to 9 power transistors in D^2PAKs mounted on thermal pads with thermal vias that extend into the ground plane, multiple QFPs, a large capacitor and transformer, SOICs of various sizes and a large number of small resistors and capacitors. The board is assembled by double-sided reflow. The 96 pin connector is soldered to the board using a paste-in-hole reflow process. Successfully attaching this connector using paste-in-hole with lead-free paste is critical. If it cannot be successfully soldered, the alternative would be adding a wave solder step to the process, which would not be cost-effective. This board is double-sided, which raises issues for the reflow process that will be discussed below. This board was selected as a test vehicle because it is of sufficient complexity to present a profiling challenge. (See Figures 5 & 6 below)

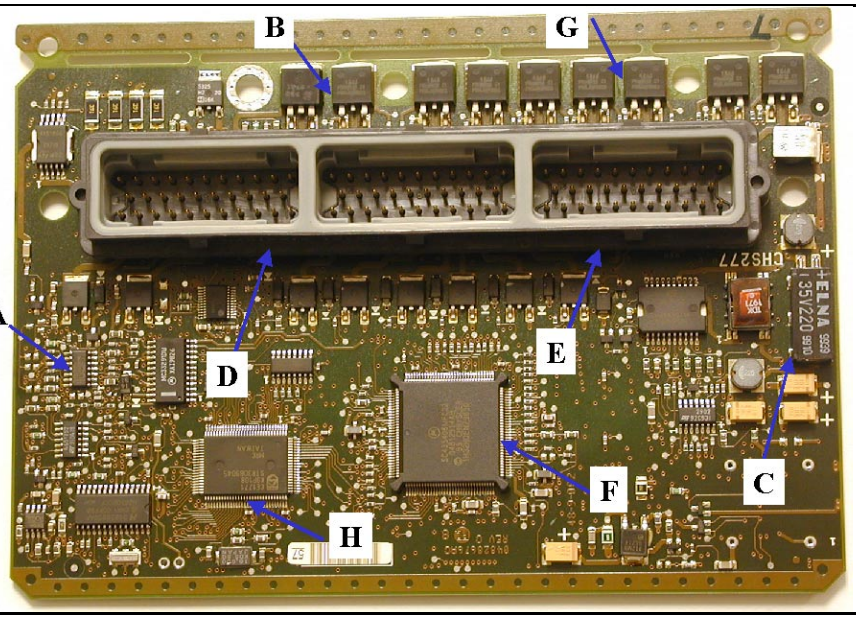
The solder alloy used to set process specification was Sn3.8Ag0.7Cu, which is commonly recognized as the most promising lead-free alloy in the United States and Europe. Process specifications were: a ramp rate of 1,5°C /sec, a reflow time (time above 217°C) of 50-70 sec, & a peak temperature of 235-240°C. This is an extremely tight process specification.

DOE

This experiment was designed to develop profiles that will successfully reflow boards of significant complexity using specifications for a common lead-free solder. The experiment was performed on a six zone solder reflow oven, and profiles were developed using automated profile prediction software.

Thermocouples were located as follows: two under the large connector—one at front and one at rear to track the leading to trailing edge temperature differential; two monitoring power transistors, two on QFP's, one on a large Capacitor, and one on a small SOIC which was the hottest point on the boards (Figures 3 & 4).

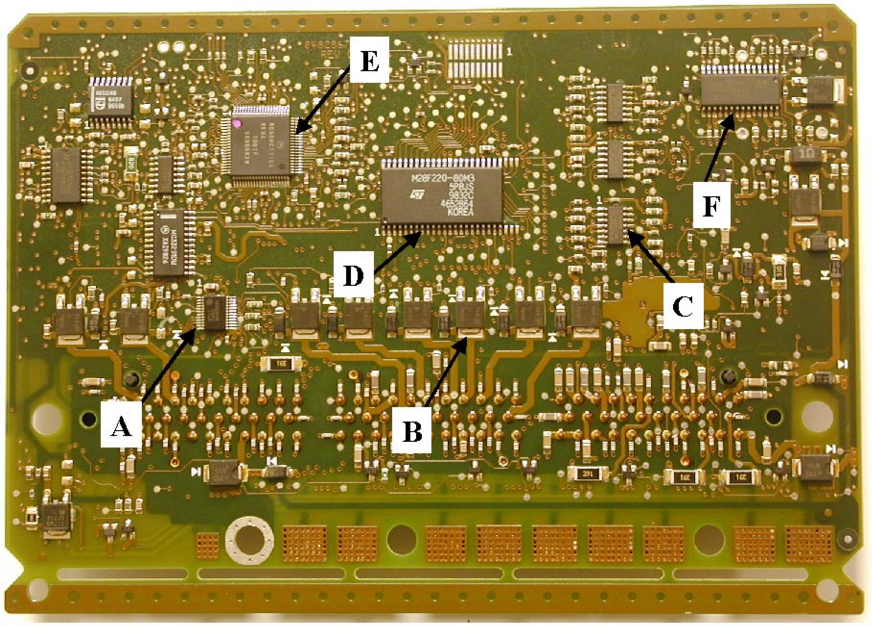
Thermocouple attachment method was to place the thermocouple bead as close to solder joint as possible and secure it with Al tape. Because the Al tape has a tendency to lift at lead-free process temperatures, a large piece of Kapton tape was placed over the Al tape.



Top Side Thermocouples

Profile	Location
■ gry-soic	A
■ red-ptr-1	B
■ blk-cap	C
■ wht-cntr	D
■ org-cntr	E
■ blu-LQFP	F
■ grn-ptr-2	G
■ vio-MQFP	H

Figure 3: Test Vehicle Top Side with Thermocouple Locations



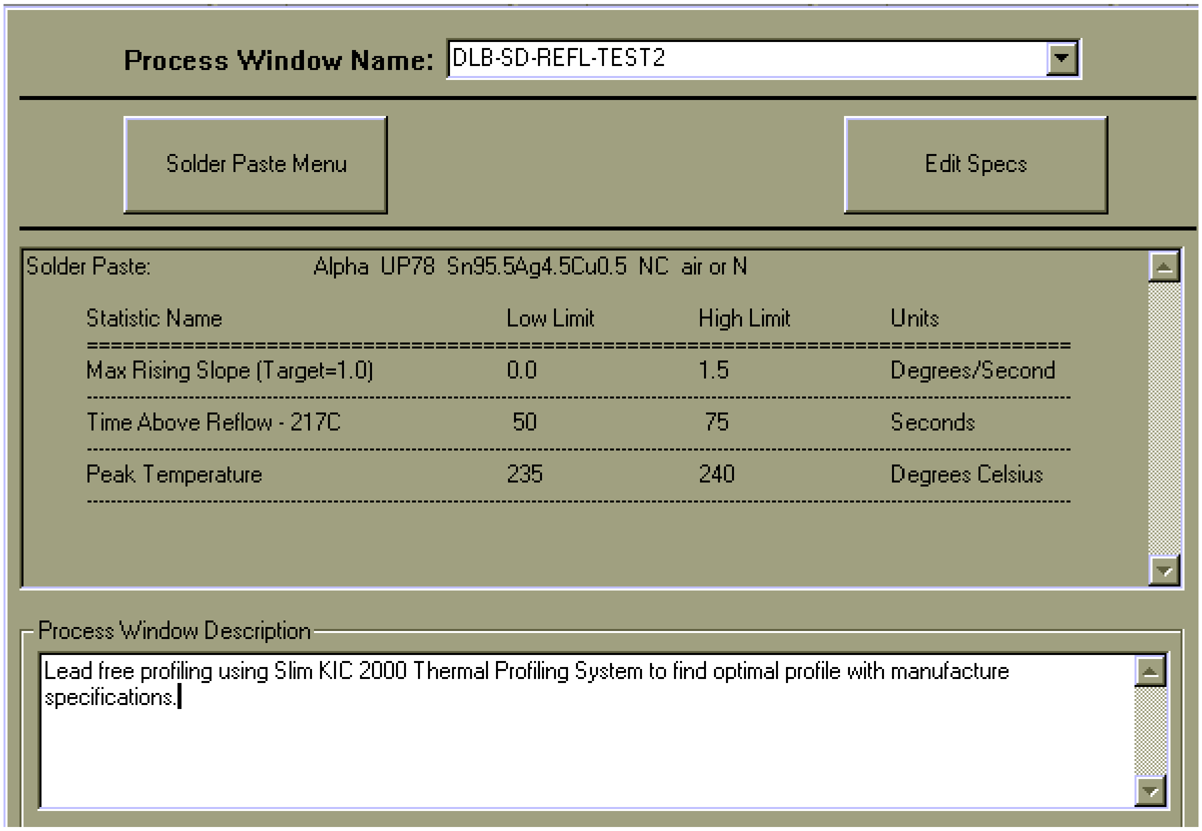
Bottom Side Thermocouples

Profile	Location
■ gry-soic-top	topside A[a]
■ Lrg-soic	D
■ ptr	B
■ Sm-soic	C
■ finepitch-soic	A
■ Med-soic	F
■ QFP	E

[a] *topsideA refers to one thermocouple placed on the topside just to compare to original topside measurements.*

Figure 4: Test Vehicle Bottom Side with Thermocouple Location

Once the test vehicle was instrumented, it was run at a "best guess" profile to develop a baseline. From this baseline, the prediction software was used to develop an optimized profile. Generally, the software is capable finding the optimal profile in two to three profiling runs. In this case, six were required to develop the optimal profile. This was because we wanted to investigate all possible options in order to assure we had the best possible profile for this assembly.



Process Window Name: DLB-SD-REFL-TEST2

Solder Paste: Alpha UP78 Sn95.5Ag4.5Cu0.5 NC air or N

Statistic Name	Low Limit	High Limit	Units
Max Rising Slope (Target=1.0)	0.0	1.5	Degrees/Second
Time Above Reflow - 217C	50	75	Seconds
Peak Temperature	235	240	Degrees Celsius

Process Window Description

Lead free profiling using Slim KIC 2000 Thermal Profiling System to find optimal profile with manufacture specifications.

Figure 5: Profile Specifications

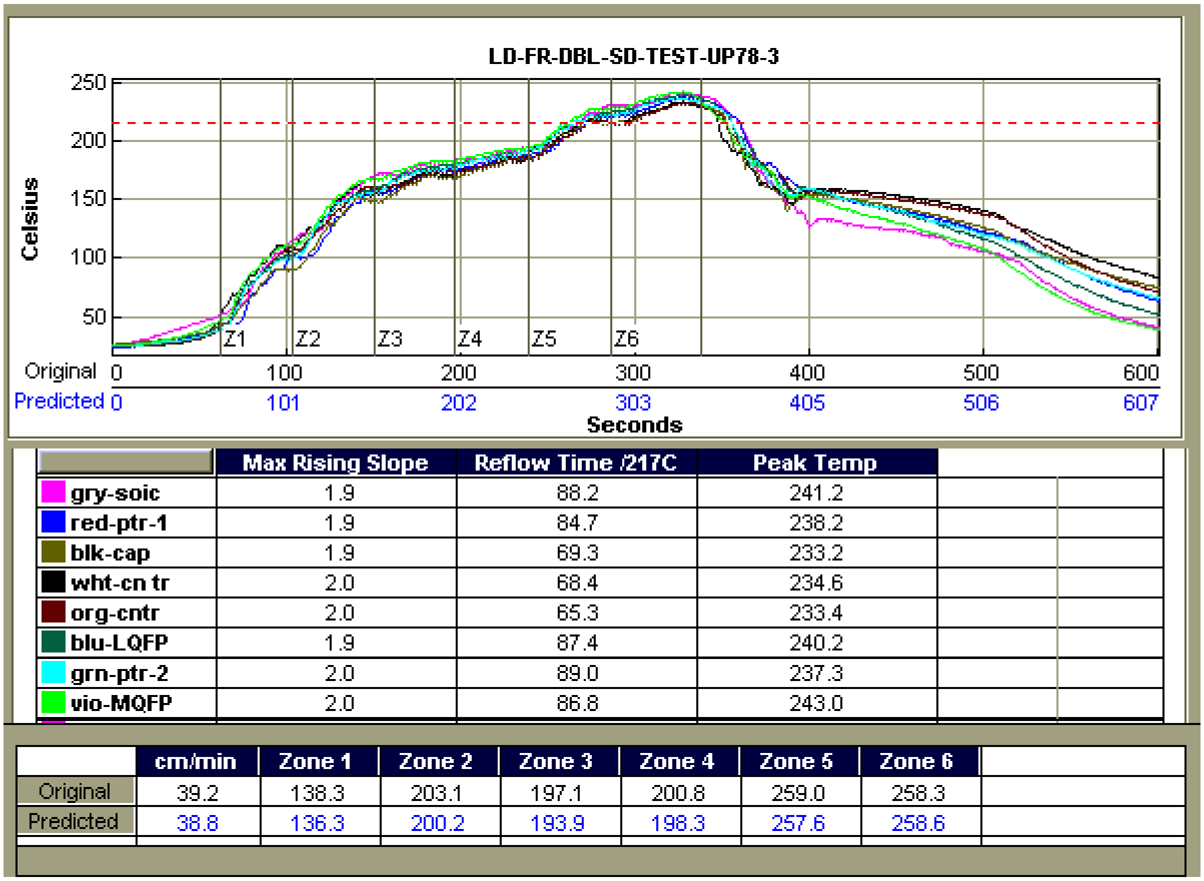
For the baseline profiling run, the board was run through the oven with the large 96 pin connector parallel to the conveyor rail. The initial profile yielded statistics of: Max Slope: 2.2-2.7 °C/sec; Reflow Time: 26.8-38.1; Peak Temperature: 230.1-254.1°C (ΔT 24.0°C). This profile was clearly unacceptable, with Max Slope exceeding specification by 1.2°C/sec; Reflow Time 23.2 sec too low; and Peak Temperature 14.1°C too high.

The second profile yielded statistics of: Max Slope: 2.2-2.5 °C/sec; Reflow Time: 56.8-101.7 sec.; Peak Temperature: 228.6-239.4°C (ΔT 10.4°C). This profile was significantly improved, though Max Slope continued exceed specification by 1.0°C/sec; and Reflow Time was now 31.7 sec too high; Peak Temperature had been brought to within 6.4 °C of spec. Especially encouraging was the reduction in ΔT to 10.8°C.

For the third run, it was decided to shift the board orientation 90° in relation to the conveyor rail, which placed the large 96 pin through-hole connector on the board's leading edge as it entered the oven. It was speculated that this orientation might block convection air flow to components "shadowed" by the connector, which were reaching too high a Peak Temperature, thus causing them to reach a lower Peak Temperature. The results of this run were: Max Slope: 1.8-2.2°C/sec; Reflow Time: 67.6-99.1 sec; Peak Temperature: 229.9-237.5°C (ΔT 7.6°C). Reorienting the board significantly improved profile, reducing Max Slope to 0.7°C in excess of specification; Reflow Time was slightly reduced to 29.1 sec too high; and Peak Temperature brought to within 5.1 °C (too low) of spec with a ΔT 7.6°C. It was now becoming clear that there were limitations to the process, and increasing Peak temperature would require increases in Reflow Time.

Further profiling runs were made to optimize the process. In runs 4-6, the automated prediction software made changes to beltspeed and oven setpoints. These changes focused on raising beltspeed and oven setpoints in an attempt to raise Peak Temperatures while lowering Reflow Time. (Note that a reduced number of profiling runs to find an optimized profile would be required in ovens with additional zones, which offer greater flexibility.)

The results of the sixth run yielded a profile that was acceptable. Statistics were: Max Slope: 1.9-2.0°C/sec; Reflow Time: 65.3-80.0 sec.; Peak Temperature: 233.2-243.0°C (ΔT 9.8°C). This profile was the best obtained for the test vehicle. Max Slope exceeded specification by 0.5°C/sec; Reflow Time was now 28.2 sec too high; and Peak Temperature had been brought to within +/-3.0 °C of spec. (Note that statistics cited above are worst case statistics for the profile.) This profile came very close to meeting the target specifications: slope was judged to be low enough to allow the flux to function properly; Reflow Time did not significantly exceed specification (though there is some question about intermetallics growth), and Peak Temperatures ensured that the assembly could be reflowed at temperatures that do not exceed component thermal stress limits. This is a significant finding: that complex assemblies can be successfully reflowed without damaging components. The final profile came close enough to the current 240°C limit to suggest that components can be reflowed in lead-free processes without significant modifications.



	Max Rising Slope	Reflow Time /217C	Peak Temp
■ gry-soic	1.9	88.2	241.2
■ red-ptr-1	1.9	84.7	238.2
■ blk-cap	1.9	69.3	233.2
■ wht-cn tr	2.0	68.4	234.6
■ org-cntr	2.0	65.3	233.4
■ blu-LQFP	1.9	87.4	240.2
■ grn-ptr-2	2.0	89.0	237.3
■ vio-MQFP	2.0	86.8	243.0

	cm/min	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5	Zone 6
Original	39.2	138.3	203.1	197.1	200.8	259.0	258.3
Predicted	38.8	136.3	200.2	193.9	198.3	257.6	258.6

Figure 6: Final Profile With Statistics

The second phase of the experiment evaluated the effect of the second reflow pass on the bottomside components attached during the first pass. The bottomside components were instrumented with thermocouples to determine whether they were being exposed to temperatures in excess of their thermal stress limits. It was found that bottomside component peak temperatures during the second reflow pass were acceptable, with a maximum peak temperature of 240.9°C, despite the higher temperatures required to reflow the denser topside components. (Figure 7)

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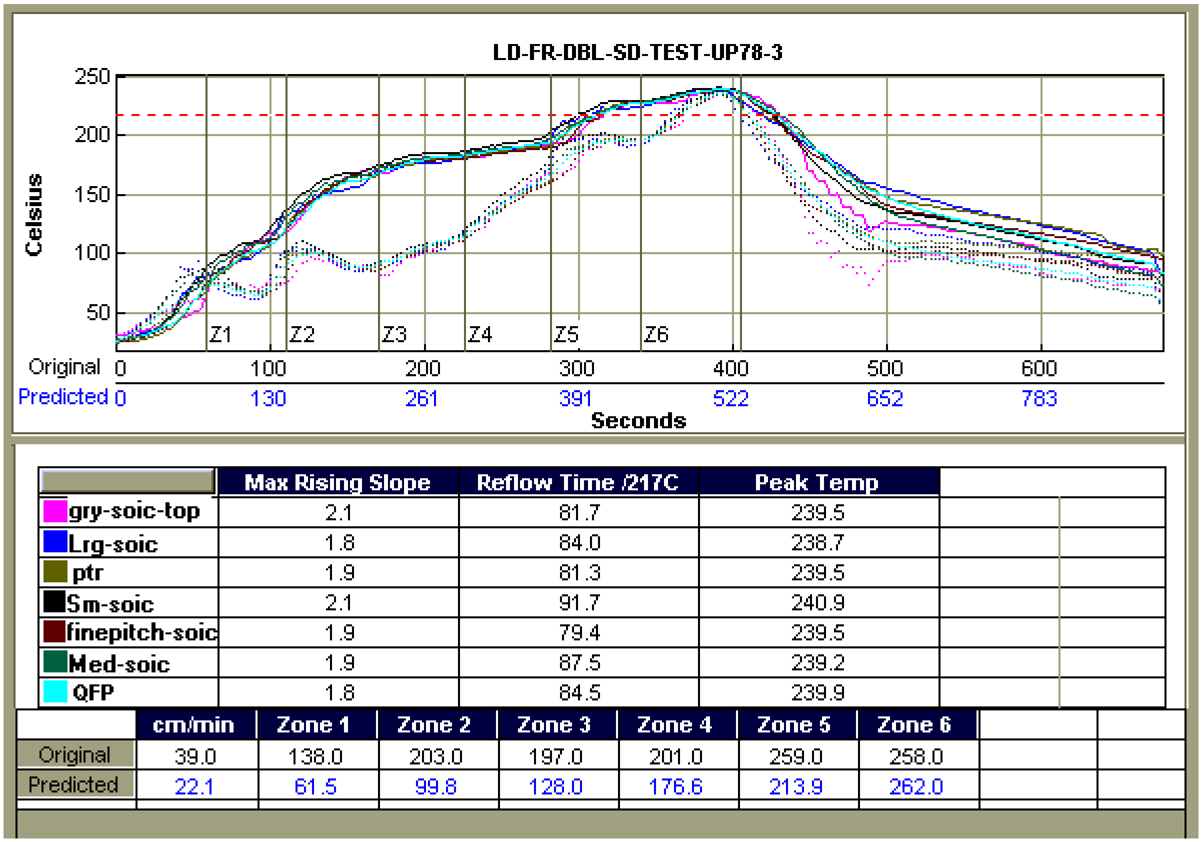

	Max Rising Slope	Reflow Time /217C	Peak Temp
■ gry-soic-top	2.1	81.7	239.5
■ Lrg-soic	1.8	84.0	238.7
■ ptr	1.9	81.3	239.5
■ Sm-soic	2.1	91.7	240.9
■ finepitch-soic	1.9	79.4	239.5
■ Med-soic	1.9	87.5	239.2
■ QFP	1.8	84.5	239.9

	cm/min	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5	Zone 6
Original	39.0	138.0	203.0	197.0	201.0	259.0	258.0
Predicted	22.1	61.5	99.8	128.0	176.6	213.9	262.0

Figure 7: Profile Monitoring Second Reflow Pass Bottomside Temperatures

As a supplement to the experiment, further tests were run on an oven with additional zones. In these tests, the automated profiling software was able to develop a profile with the following profile statistics: Max Slope: 1.1-1.2°C/sec; Reflow Time: 47.9-58.0 sec; Peak Temperature: 233.7-240.6°C (ΔT 6.9°C). This profile was the best obtained for the test vehicle. Max Slope was within spec, as was Reflow Time. Peak Temperature was brought to within +/-1.3°C of spec. This profile came even closer than the final profile (above) to meeting the target specifications, with only Peak Temperature being slightly out on a very tight profile spec. This supplemental work suggests that the number of oven zones is an important factor in developing lead-free reflow processes.

Test Results

The optimal process profile developed reached the physical limits of the process, and engineers were forced to choose between reducing Reflow Time to meet the solder paste spec, or reducing Peak Temperatures to meet the component thermal stress specs. The automated prediction software delivered the best possible profile for this test vehicle—a profile that reduced the ΔT from a first pass high of ΔT 24°C with a totally unacceptable profile to ΔT 9.8°C with a profile that would produce good quality solder joints without damaging sensitive components. The profile also met the wetting specification for the solder paste. The profile also achieved a good temperature spread across the board. Some points on the board are a little over the Reflow Time, but this time can be reduced by increasing the Peak ΔT across the board. Conversely, by extending Reflow Time, board temperatures will stabilize and reduce the Peak ΔT. This is the result of natural process limitations. The automated prediction software is capable of finding a profile that will reach the alternate spec, but it cannot develop a profile that is better than the thermal limitations of the process. With complex assemblies compromises may have to be made, chiefly between limiting component thermal stress and ensuring long term solder joint reliability by limiting the growth of intermetalics. Additional trade-offs occur in the Peak Temperature—the choice is between increased wetting and limiting thermal stress on components.

Conclusions

Automated profile prediction software provides significant benefits for developing reflow profiles for lead-free electronics assembly. In the case of this experiment, the automated profiling tool came close to meeting all of the target specs, which were set very tight to test the tool's capability to minimize ΔT's across complex assemblies. This experiment has established that lead-free electronic assemblies can be successfully reflowed in a reduced process window, thus offering the potential to limit the impact of the transition to higher temperature lead-free processes, especially in terms of raising component thermal stress limits.

Other findings were:

- SnAgCu wets adequately on PWB surface finishes at 230°C. (The F_{max} for OSP offers marginal spreading at 230°C.) Optimal wetting is achieved at temperatures of 235°C, and temperatures over 240°C do not significantly increase wetting.
- Board orientation in the oven can affect the thermal profile. As reorienting the board has obvious negative effects on productivity and throughput, it should only be considered as a last option.
- In double-sided reflow processes, bottomside temperatures should monitored to ensure that bottom-side components are not exceeding their thermal stress limits during the second reflow pass.

The previous method of profiling at this facility involved using a datalogger, attaching T/Cs to the assembly, running profile, then making an educated guess as to what had to be done next —in essence, the status quo method described on Page 4. Based on previous experience, it would have taken at least two to three times as long to have developed the profile using human process experience as opposed to developing the profile with automated prediction software. The automated prediction tool makes profiling a science, rather than an art, and this will have a significant impact on the implementation of lead-free processes.

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